IN THE CLAIMS:

1. (Previously Presented) A digital system that comprises:

a plurality of units operating at a first clock rate, each unit configured to independently process a sequence of data items; and

a domain crossover element configured to receive a stream of data items at a second clock rate different from the first clock rate and configured to distribute separate sequences of data items through separate ports to the plurality of units.

2. (Original) The system of claim 1, wherein the second clock rate is greater than the first clock rate, and wherein the number of ports equals a positive integer multiple of the ratio of the second clock rate to the first clock rate.

3. (Original) The system of claim 2, wherein said number of ports is two.

4. (Original) The system of claim 1, wherein the units are general purpose processors.

5. (Original) The system of claim 1, wherein the data items are data packets having fields for a packetID, a targetID, Control flags, and packet Data.

6. (Original) The system of claim 1, wherein the domain crossover element includes a circular buffer having a plurality of distinct sections each associated with a corresponding one of the separate ports, and each having N storage locations, where N is a positive integer.

7. (Original) The system of claim 6, wherein each of said separate sequences of data items is formed by repeatedly reading from sequential storage locations in a corresponding section of the circular buffer.

8. (Original) The system of claim 6, wherein N is two or greater.

9. (Original) The system of claim 7, wherein N is four.

10. (Original) The system of claim 1, wherein the domain crossover element comprises:

a counter/decoder that receives an input clock and responsively asserts sequential ones of a plurality of output signals;

a plurality of storage location registers, each coupled to receive corresponding one of the plurality of output signals from the counter/decoder, and each coupled to receive a stream of input data items, wherein each of the storage location registers is configured to store an input data item when the corresponding one of the plurality of output signals is asserted;

a plurality of multiplexers each configured to provide a sequence of data items to one of the separate ports, wherein each of the multiplexers is coupled to storage location registers associated with said one of the separate ports; and

an output counter that receives an output clock, wherein the output counter is coupled to one or more of the multiplexers and configured to sequentially select storage locations for the one or more multiplexers to access to provide said sequences of data items.

11. (Original) A domain crossover element that comprises:

an input counter that receives an input clock;

a plurality of storage location registers that are sequentially selected by the input counter and configured to store a data item from an input stream when selected;

an output counter that receives an output clock having a slower clock rate than the input clock;

a first multiplexer having inputs that are sequentially selected by the output counter, wherein the inputs of the first multiplexer are coupled to

respective storage location registers in a first subset of the plurality storage location registers; and

a second multiplexer having inputs that are sequentially selected by the output counter, wherein the inputs of the second multiplexer are coupled to respective storage locations in a second subset of the plurality of storage location registers, wherein the second subset is distinct from the first subset.

12. (Original) The domain crossover element of claim 11, further comprising:

a set of logic gates that shifts selected inputs of the second multiplexer relative to the selected inputs of the first multiplexer.

13. (Original) The domain crossover element of claim 11, further comprising:

a validity latch that is de-asserted upon initialization, and that becomes asserted once at least one of the storage location registers in the second subset has stored a data item from the input stream.

14. (Original) The domain crossover element of claim 13, wherein the validity latch's state is used to gate a clock signal associated with output from the second multiplexer.

15. (Original) The domain crossover element of claim 11, wherein the plurality of storage location registers includes eight storage location registers, and wherein the first subset includes the first four storage location registers, and the second subset includes the second four storage location registers.

16. (Original) The domain crossover element of claim 11, wherein each of the plurality of storage location registers has an associated validity register that indicates if the corresponding storage location register has been written and not read.

17. (Original) A method of distributing a stream of data items received at a first clock rate among a plurality of processing units operating at a second, slower clock rate, the method comprising:

sequentially selecting one of a plurality of registers at the first clock rate;

storing each data item from the stream of data items in a selected register as the data items are received;

sequentially selecting one of a first subset of the plurality of registers at the second clock rate;

sequentially selecting one of a second subset of the plurality of registers at the second clock rate, wherein the second subset is distinct from the first subset; and

concurrently reading data items from the selected ones of the first and second subsets at the second clock rate.

18. (Original) The method of claim 17, wherein the first data item read from the first subset is read at a different time than the first data item read from the second subset.

19. (Original) The method of claim 17, wherein all registers in the second subset are written after all registers in the first subset.

20. (Original) The method of claim 17, further comprising:

continuously repeating the acts of claim 17 while a reset signal is de-asserted